

# CETPA INFOTECH PVT. LTD.

## CURRICULUM OF SYSTEM VERILOG HVL

### ASIC verification methodologies

- Directed Vs random
- Functional verification process
- Stimulus generation
- Bus functional model
- Monitors and reference models
- Coverage driven verification
- Verification planning and management
- Typical Verification Environment

### System Verilog Introduction

- Hardware Description Languages (HDLs)
- Flavors of System Verilog
- Language Basics Outline

### Different Data Types

- Casting
- String
  - ❖ String Methods
- User-defined Data Types
  - ❖ Structure
  - ❖ Union
  - ❖ Enumeration
    - Enum Methods
      - Type Day
- Arrays
  - ❖ Packed
  - ❖ Unpacked
  - ❖ Fixed Size Array
  - ❖ Array Dynamic
    - Dynamic Array Methods
  - ❖ Associative Array
    - Associative Array Methods
  - ❖ Array Methods
- Queues
  - ❖ Queues Methods

### Procedural Statement

- Conditional Statement
  - ❖ If else statement
  - ❖ Case statement
- Iteration Methods
  - ❖ for loop
  - ❖ while loop
  - ❖ do while loop
  - ❖ forever loop
  - ❖ repeat

- Task and Function

### Features of Verification

- Interface
- Clocking Block
- Program Block
- MODPORT
- OOPs
  - ❖ Terminology
    - Class
    - Object
    - Handle
    - Properties
    - Method
  - ❖ Class routine
  - ❖ Inheritance
  - ❖ Polymorphism
  - ❖ Abstraction
  - ❖ Encapsulation
- Inter Process Communication
  - ❖ Working with threads
  - ❖ Flavours of fork join
  - ❖ Semaphores
    - Semaphores Method
  - ❖ Mail Box
    - Mailbox Methods
- Randomization
  - ❖ Randomization function
  - ❖ Types of randomization
  - ❖ Random Constraints
- Assertions
  - ❖ Concurrent assertions
  - ❖ Immediate assertions
  - ❖ Property block
  - ❖ Sequence block
  - ❖ Assert, Assume and Cover
- Coverage
  - ❖ Coverage type
  - ❖ Coverage Strategy
  - ❖ Coverage model
  - ❖ Coverage points
  - ❖ Cross Coverage
  - ❖ Functional Coverage

### Project Work

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