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Curriculum Of System Verilog HDL

Duration: 6 Weeks

ASIC VERIFICATION METHODOLOGIES
- Directed Vs random
- Functional verification process
- Stimulus generation
- Bus functional model
- Monitors and reference models
- Coverage driven verification
- Verification planning and management

SYSTEM VERILOG INTRODUCTION
- Hardware Description Languages (HDLs)
- Flavors of System Verilog
- Language Basics Outline

DIFFERENT DATA TYPES
- Casting
- String
  - ❖ String Methods
- User-defined Data Types
  - ❖ Structure
  - ❖ Union
  - ❖ Enumeration
- Arrays
  - ❖ Packed
  - ❖ Unpacked
  - ❖ Fixed Size Array
  - ❖ Dynamic
  - ❖ Associative Array
  - ❖ Array Methods
- Queues
  - ❖ Queues Methods

PROCEDURAL STATEMENT
- Conditional Statement
  - ❖ If else statement
  - ❖ Case statement
- Iteration Methods
  - ❖ for loop
  - ❖ while loop
  - ❖ do while loop
  - ❖ forever loop
  - ❖ repeat
- Task and Function

FEATURES OF VERIFICATION
- Interface
- Clocking Block
- Program Block
- OOPs
  - ❖ Terminology
    - ▪ Class
    - ▪ Object
    - ▪ Handle
    - ▪ Properties
    - ▪ Method
  - ❖ Class routine
  - ❖ Inheritance
  - ❖ Polymorphism
  - ❖ Virtual Class
- Inter Process Communication
  - ❖ Working with threads
  - ❖ Types of fork join
  - ❖ Semaphores
  - ❖ Mail Box
- Randomization
  - ❖ Randomization function
  - ❖ Types of randomization
  - ❖ Random Constraints
- Assertions
  - ❖ Concurrent assertions
  - ❖ Immediate assertions
  - ❖ Property block
  - ❖ Sequence block

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- ❖ Assert, Assume and Cover

• Coverage
- ❖ Coverage type
- ❖ Coverage Strategy
- ❖ Coverage model
- ❖ Coverage points
- ❖ Cross Coverage

PROJECT WORK