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Curriculum Of Verilog HDL

Duration: 6 Weeks

INTRODUCTION TO VLSI
- Need, Scope, Use and History of VLSI
- Introduction to Chip Design Process
- Description of Hardware Description Languages
- Applications of VLSI
- Evolution of Computer Aided Digital Design
- Emergence of HDL's
- VLSI Design Flow.
- Importance of HDL's.

INTRODUCTION TO VERILOG HDL
- Need, Scope, Use and History of Verilog HDL
- Special Features of Verilog HDL
- Application of Verilog HDL in Market and Industries
- Discussion of Verilog HDL & other procedural language.

DESIGNING IN VERILOG HDL
- Design Methodology
  - ❖ Top-Down Methodology
  - ❖ Bottom-up Methodology
- Design Simulation and Design Synthesis
- Verilog HDL Design Flow
- Keyword description in VERILOG HDL
  - ❖ Module Description

DATA TYPES IN VERILOG HDL
- Lexical Conventions
- Description of Data types
  - ❖ Net
  - ❖ Register
- Scalar Data Description
- Vector Data Description
- Parameters Description
- Array Description

INTRODUCTION OF DIFFERENT MODELING STYLE
- Gate level Modeling
- Dataflow modeling
- Behavioral Modeling
- Switch level Modeling

GATE LEVEL MODELING
- Logic Gate Primitive
- Gate Instantiation
- Design RTL from Logic Diagram
- Delays in Gate-Level Design
  - ❖ Rise Delay
  - ❖ Fall Delay
  - ❖ Turn off Delay

DATAFLOW MODELING
- Continuous Assignment statement
- Implicit Assignment statement
- Delay
  - ❖ Assignment Delay
  - ❖ Implicit Assignment Delay
  - ❖ Net declaration Delay
- Expressions
- Basic Operators
- Verilog specific operators (Case equality etc.)
- Operands
- Operator Precedence

BEHAVIORAL MODELING
- Structured Procedural Statements
  - ❖ Always Statements
  - ❖ Initial Statements
- Blocking Statement
- Non blocking Statement
- Timing Control Statement
  - ❖ Delay Based Timing Control

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- ❖ Event Based Timing Control
- Conditional statements
  - ❖ If-else statements
  - ❖ Case statements
- Loops
  - ❖ While loop
  - ❖ For loop
  - ❖ Repeat loop
  - ❖ Forever loop
- Block Statements
  - ❖ Parallel block
  - ❖ Sequential block

FINITE STATE MACHINE (FSM)

- Introduction to FSM
- Mealy Machine
- Moore Machine
- Flip-flops
- Counters

MINOR PROJECTS

- TLC by Sensors
- TLC four way based on timing control
- ALU Design
- Shift unit Design
  - ❖ LFSR (Linear Feedback Shift Register)
  - ❖ MISR (Multiple Input Signature Register)
- Booth Multiplier
- Wallace Multiplier
- Comparator Unit Design

HARDWARE IMPLEMENTATION

- Introduction to FPGA
- Introduction to CPLD
- Brief discussion of Hardware kit
- Working on Physical FPGA and CPLD
- LED Interfacing
- 7-segment interfacing
- LCD Interfacing
- Keypad Scanner
- Clock Divider RTL Code

USEFUL MODELING TECHNIQUE

- Procedural Continuous Assignment Statement
  - ❖ Assign Statement
  - ❖ Deassign Statement
  - ❖ Force Statement
  - ❖ Release Statement
- Defparam Statement
- Switch level Modeling style
  - ❖ MOS Switches
  - ❖ Bidirectional Pass Switches.
  - ❖ Resistive MOS Switches
- Introduction to system Verilog
- Sub Programs
- Tasks
- Functions
- Difference between Tasks and Functions
- Understanding of Automatic keyword in Tasks and Functions
- User Defined Primitives (UDP's)
  - ❖ Combinational UDP'S
  - ❖ Sequential UDP'S.
- Verilog Test bench
- Test Bench for Combinational Design
- Test Bench for Sequential Design
- Sequential Block (Begin-end)
- Parallel Block (Fork –Join)
- Logic synthesis
- System Task
  - ❖ $display
  - ❖ $monitor
  - ❖ $finish
  - ❖ $stop
  - ❖ $random
- Compiler Directives

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Curriculum Of Verilog HDL

- `define
- `include
- `ifdef

'

- ifndef
- `timescale

MEMORY MODELING

- AM & ROM designing
- Bi - directional ports
- Case X and Case Z statements

MAJOR PROJECTS

Project list mentioned on--
http://www.cetpainfotech.com